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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,611	10/06/2000	Guy Meynants	16820.P376	3244

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EXAMINER	
JONES, HEATHER RAE	
ART UNIT	**PAPER NUMBER**
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/684,611	MEYNANTS, GUY	
	Examiner	Art Unit	
	Heather R. Jones	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-12,17,19-24 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-12,17,19-24 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 5-12, 17, 19-24, and 27-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim1, 2, 5-12, 17, 19-24, and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx et al. (WO 99/16238).

Regarding claim **1**, Dierickx et al. discloses in Fig. 2 an amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal; a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-9); at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element; a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27); an input switching element disposed on each connecting line (S41 and S51; or S61),

between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element; at least one output switching element (X1) coupled to the output terminal of the amplifying element (A1); a first readout bus (Y) coupled to the least one output switching element (X1); a second readout bus coupled to at least one output element (the second readout bus can be seen as the bottom line in Fig. 3, which is reference character "D" blown up); and an output amplifier coupled to the first and second readout buses (the output amplifier can be seen in Fig. 3 along with both the first and second readout buses).

Regarding claim **2**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 as well as disclosing that the amplifying circuit comprises a memory element on each of the connecting lines (MR1 and MS1).

Regarding claim **5**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors. (It is inherent that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors).

Regarding claim **6**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element

is an operational transconductance amplifier (It is inherent that the amplifying element is an operational transconductance amplifier).

Regarding claim **7**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the memory element is a capacitor (page 11, lines 20-21 and 27).

Regarding claim **8**, Dierickx et al. discloses in Fig. 2 an array of amplifying circuits, each amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal; a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-9); at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element; a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27); a switching element disposed on each connecting line (S41 and S51; or S61), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element; a first output switching element (X1) coupled to the output terminal of the amplifying element (A1); a second output switching element coupled to the output terminal of the amplifying element (the second output switching element can be seen in Fig. 3); a first readout bus

(Y) coupled to the first output switching element (X1); a second readout bus coupled to the second output switching element (the second readout bus can be seen as the bottom line in Fig. 3, which is reference character "D" blown up); and an output amplifier coupled to the first and second readout buses (the output amplifier can be seen in Fig. 3 along with both the first and second readout buses), wherein the first and second readout buses are coupled to each of the array of amplifying circuits (as can be seen in Fig. 2).

Regarding claim **9**, Dierickx discloses in Fig. 2 a device for imaging applications, comprising: a matrix of active pixels arranged in a geometric configuration, each pixel producing an electrical signal indicative of the light intensity of a portion of a scene being imaged by that pixel (page 1, lines 25-32), at least one amplifying circuit common to a group of pixels out of the matrix, wherein each amplifying circuit comprises an amplifying element (A1) with at least an input terminal and an output terminal; a signal input node (I1) being intended to obtain electrical signals from pixels out of the group of pixels to which the amplifying circuit is common, the signal levels of are to be amplified by the amplifying element (page 11, lines 6-9); at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring an electrical signal from the signal input node to the input terminal of the amplifying element; a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the electrical signals at the signal input node at a moment in time (Page 11, lines 15-27); a switching

element disposed on each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line (S41 and S51), for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element; at least one output switching element (X1) coupled to the output terminal of the amplifying element (A1); a first readout bus (Y) coupled to the least one output switching element (X1); a second readout bus coupled to at least one output element (the second readout bus can be seen as the bottom line in Fig. 3, which is reference character "D" blown up); and an output amplifier coupled to the first and second readout buses (the output amplifier can be seen in Fig. 3 along with both the first and second readout buses), wherein the first and second readout buses are coupled to each amplifying circuit (as can be seen in Fig. 3).

Regarding claim **10**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a row of pixels (Fig. 2).

Regarding claim **11**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a column of pixels (Fig. 2).

Regarding claim **12**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the first and second

readout buses are common to the matrix of active pixels (as can be seen in Fig. 2).

Regarding claim **17**, Dierickx et al. discloses a method for reducing fixed pattern noise of solid state imaging device having a group of active pixels (page 4, lines 30-35), each pixel comprising a radiation sensitive element (page 1, lines 25-32) and an amplifying circuit, the method comprising: reading out the signal of a pixel brought in a first state and storing the corresponding voltage level in a first memory element, reading out the signal of the pixel brought in a second state, which is different from the first state, and storing the corresponding voltage level in a second memory element (page 11, lines 15-28), transferring the signal of the first memory element to an amplifying element, amplifying it and transferring it to a first readout bus; transferring the signal of the second memory element to the same amplifying element, amplifying it and transferring it to a second readout bus (page 10, line 29 – page 11, line 5); and repeating these steps for at least part of the pixels of the imaging device (page 11, line 29 – page 12, line 8).

Regarding claim **19**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 as well as disclosing that it further comprises the step of calculating a differential output signal by taking the difference between potential values on the first and second readout buses (page 3, lines 10-23).

Regarding claim **20**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the first state and the

second state correspond to different amounts of radiation collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **21**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the first state or second state corresponds to an amount of radiation or light collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **22**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the second state or the first state corresponds to a non-irradiated or non-illuminated or dark or reset state of the pixel (page 11, lines 15-28).

Regarding claim **23**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the pixel is read out in additional states and its corresponding voltage level is being stored on additional memory elements (page 1, line 25 – page 4 lines 7; page 11, lines 6 – page 12, line 20).

Regarding claim **24**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the signal of the first memory element is transferred to the first output line common for the group, and concurrently, the signal of the second memory element of another amplifier is transferred to the second output line common for the group (Fig. 3).

Regarding claim **27**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the first readout bus is

a signal bus and the second readout bus is a reset bus (page 10, line 29 – page 11, line 5).

Regarding claim **28**, Dierickx et al. discloses all the limitations as previously discussed with respect to claims 1 and 27 including that the output amplifier has a positive input and a negative input and wherein the signal bus is coupled to the positive input and the reset bus is coupled to the negative input (as can be seen Fig. 3).

Regarding claim **29**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that a differential signal on the first and second readout buses is proportional to the signal levels of the signal input node (page 10, line 29 – page 11, line 5).

Regarding claim **30**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the at least one switching element comprises: a first output switching element (X1) coupled to the output terminal of the amplifying element; and a second output switching element (as can be seen in Fig. 3) coupled to the output terminal of the amplifying element, and wherein the first readout bus is coupled to the first output switching element and the second readout bus is coupled to the second output switching element (as can be seen in Fig. 3).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather R. Jones whose telephone number is 571-272-7368. The examiner can normally be reached on Mon. - Thurs.: 7:00 am - 4:30 pm, and every other Fri.: 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached on 571-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Heather R Jones
Examiner
Art Unit 2621

HRJ
October 16, 2006

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